

HVV1012-060

New Product Qualification

Date: May 15, 2010

# HVV1012-060 Reliability Qualification Report

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## Purpose

This report qualifies the HVV1012-060. The die is fabricated at ON Semiconductor's COM1 facility in Phoenix, Arizona. The package is assembled at the HVVi<sup>®</sup> assembly site in Phoenix, Arizona.

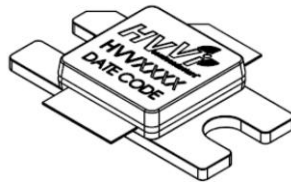
## Background Information

The HVV1012-060 device is a high voltage silicon enhancement mode RF transistor designed for L-Band pulsed avionics applications operating in the frequency range of 1025MHz to 1150MHz. It is rated at 60 Watts. The device features high power gain, excellent ruggedness, and a 50V supply voltage. Table 1 provides a description of the device.

The qualification consisted of three wafer lots which were fabricated at ON Semiconductor's COM1 facility in Phoenix, Arizona. Multiple assembly lots were manufactured at HVVi in Phoenix, Arizona. The reliability stress tests were performed per industry standards (JEDEC, AEC, and MIL-STD-883). Reliability stress tests were performed at HVVi Semiconductors, Inc.

**Table 1.** General device description of the HVV1012-060.

<b>Device</b>	HVV1012-060	<b>Wafer Fab Site</b>	ON Semiconductor, COM1	Phoenix, Arizona
<b>Package</b>	HV400	<b>Assembly Site</b>	HVVi	Phoenix, Arizona
<b>Technology</b>	HVVFET™	<b>Final Test Site</b>	HVVi	Phoenix, Arizona



**Figure 1.** Package drawing of the HVV1012-060.

**Table 2.** List of reliability lab companies, locations, and tests performed.

<b>Reliability Lab</b>	<b>Location</b>	<b>Tests Completed</b>
HVVi Semiconductors, Inc.	Phoenix, Arizona	Temperature Cycling

## Qualification Tests and Results

The qualification tests were performed per standard test conditions (JEDEC, AEC-101, MIL-STD-883). Sample sizes were chosen per recommended sizes or per Lot Tolerance Percent Defective (LTPD) Sampling based on the Military Standards (5% level).

**Table 3.** A list of reliability tests completed for the HVV1011-300 qualification.

Stress	Abbv.	Ref.	Conditions	Duration/ Acceptance	Lot A	Lot B	Lot C
Electrical Parameter Assessment	ED	JESD86	Datasheet	Per datasheet	All	All	All
Temperature Cycling	TC	JESD22-A104	-40 °C to +125 °C	1000 cycles / 0 Fail	0/45	0/45	0/45

## Explanation of Tests

**Stress Test/Specification: Temperature Cycling (TC)/JESD22-A104**

**Conditions:** Ta = -40 °C to +125 °C; unbiased

**Read Points:** 0 and 1000 cycles

**Sample Size:** 3 lots, 45 units each (per LTPD 5% level with no failures)

**Purpose:** Accelerate failure mechanisms caused by cycling between high and low temperatures.

**Possible Failure Mechanisms/Modes:** Failure mechanisms include fatigue and cracking related failures such as broken bonds or cracked die due to stresses caused by thermal mismatches in Coefficients of Thermal Expansion (CTE). Failure modes include degradation of thermal and electrical characteristics and catastrophic failure. Thermal and electrical parameters affected include R<sub>dson</sub>, R(θ)<sub>JC</sub>, V<sub>dss</sub>, and V<sub>gs</sub>.

## Qualification by Similarity

The HVV1012-060 device is qualified by similarity from the HVV1011-300 based on similarity in wafer technology and die (High Temperature Reverse Bias, High Temperature Gate Bias, Unbiased Highly Accelerated Stress Test), and based on similarity in fabrication, assembly manufacturing, and materials (Solderability, Resistance to Solder Heat, Vibration Variable Frequency, Mechanical Shock, Constant Acceleration).

## Summary

The reliability test results documented herein qualify the HVV1012-060 device. The die is supplied by ON Semiconductor's COM1 facility in Phoenix, Arizona and the package is assembled at HVVi in Phoenix, Arizona. The HVV1012-060 device meets or exceeds HVVi's requirements for product reliability.

