HVV1011-600

New Product and Package Qualification

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HVV1011-600 Reliability Qualification Report

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Purpose

This report qualifies the HVV1011-600. The die is fabricated at ON Semiconductor's COM1 facility in Phoenix, Arizona. The package is assembled at the HVVi® assembly site in Phoenix, Arizona.

Background Information

The HVV1011-600 device is a high voltage silicon enhancement mode RF transistor designed for L-Band pulsed avionics applications operating in the frequency range of 1030MHz to 1090MHz. It is rated at 600 Watts. The device features high power gain, excellent ruggedness, and a 50V supply voltage. Table 1 provides a description of the device.

The HVV1011-600 device qualifies by similarity from the HVV1011-300 based on similarity in wafer technology and die (High Temperature Reverse Bias, High Temperature Gate Bias, Unbiased Highly Accelerated Stress Test), and based on similarity in fabrication, assembly manufacturing, and materials (Solderability, Resistance to Solder Heat, Vibration Variable Frequency, Mechanical Shock, Constant Acceleration).

The qualification consisted of three wafer lots which were fabricated at ON Semiconductor's COM1 facility in Phoenix, Arizona. Multiple assembly lots were manufactured at HVVi in Phoenix, Arizona. The reliability stress tests were performed per industry standards (JEDEC, AEC, and MIL-STD-883). Reliability stress tests were performed at HVVi Semiconductors, Inc.

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Table 1. General device description of the HVV1011-600.

Device	HVV1011-600		**Wafer Fab Site**	ON Semiconductor, COM1	Phoenix, Arizona
Package	HV800		**Assembly Site**	HVVi	Phoenix, Arizona
Technology	HVVFET™		**Final Test Site**	HVVi	Phoenix, Arizona

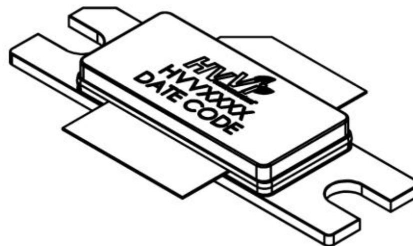

Figure 1. Package drawing of the HVV1011-600.

Qualification Tests and Results

Table 2. List of reliability lab companies, locations, and tests performed.

Reliability Lab	Location	Tests Completed
HVVi Semiconductors, Inc.	Phoenix, Arizona	Temperature Cycling

The qualification tests were performed per standard test conditions (JEDEC, AEC-101, MIL-STD-883). Sample sizes were chosen per recommended sizes or per Lot Tolerance Percent Defective (LTPD) Sampling based on the Military Standards (5% level).

Table 3. A list of reliability tests completed for the HVV1011-300 qualification.

Stress	Abbv.	Ref.	Conditions	Duration/ Acceptance	Lot A	Lot B	Lot C
Electrical Parameter Assessment	ED	JESD86	Datasheet	Per datasheet	All	All	All
Temperature Cycling	TC	JESD22-A104	-40 °C to +125 °C	1000 cycles / 0 Fail	0/45	0/45	0/45

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Explanation of Tests

Stress Test/Specification: Temperature Cycling (TC)/JESD22-A104
Conditions: Ta = -40 °C to +125 °C; unbiased
Read Points: 0 and 1000 cycles
Sample Size: 3 lots, 45 units each (per LTPD 5% level with no failures)
Purpose: Accelerate failure mechanisms caused by cycling between high and low temperatures.
Possible Failure Mechanisms/Modes: Failure mechanisms include fatigue and cracking related failures such as broken bonds or cracked die due to stresses caused by thermal mismatches in Coefficients of Thermal Expansion (CTE). Failure modes include degradation of thermal and electrical characteristics and catastrophic failure. Thermal and electrical parameters affected include Rdson, R(θ)jC, Vdss, and Vgs.

Qualification by Similarity

The following devices are qualified by similarity to the HVV1011-600 based on the similarity in wafer technology, fabrication, die size, assembly manufacturing, and materials:

HVV1012-550, HVV0708-600.

Summary

The reliability test results documented herein qualify the HVV1011-600 in the HV800 package. The die is supplied by ON Semiconductor’s COM1 facility in Phoenix, Arizona and the package is assembled at HVVi in Phoenix, Arizona. The HVV1011-600 device meets or exceeds HVVi’s requirements for product reliability.