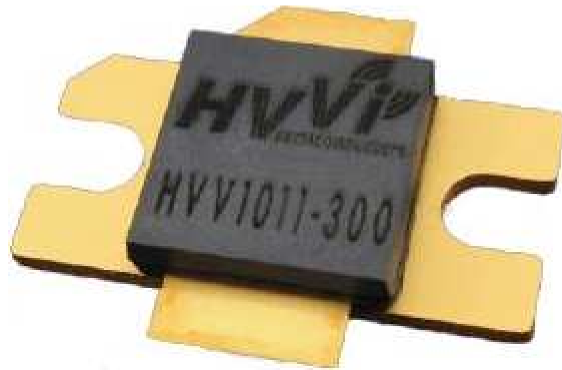

HVV1011-300
New Product Qualification

December 5, 2008

HVV1011-300 Reliability Qualification Report

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Purpose

This report qualifies the HVV1011-300 device and the HV400 package. The die is fabricated at ON Semiconductor's COM1 facility in Phoenix, Arizona. The package is assembled at the HVVi® assembly site in Phoenix, Arizona.

Background Information

The high power HVV1011-300 device is a high voltage silicon enhancement mode RF transistor designed for L-Band pulsed avionics applications operating over the frequency range from 1030MHz to 1090MHz. It is rated at 300 Watts. The device features high power gain, excellent ruggedness and a 48V supply voltage. Table 1 provides a description of the device.

The qualification consisted of three wafer lots which were fabricated at ON Semiconductor's COM1 facility in Phoenix, Arizona. Multiple assembly lots were manufactured at HVVi in Phoenix, Arizona. The reliability stress tests were performed per industry standards (JEDEC, AEC, and MIL-STD-883). Reliability stress tests were performed at three different locations. The reliability facilities used were ON Semiconductor's Reliability Lab, EAG/White Mountain Labs, and Silicon Cert, Ltd as detailed in Table 2.

Table 1. General device description of the HVV1011-300.

Device	HVV1011-300		**Wafer Fab Site**	ON Semiconductor, COM1	Phoenix, Arizona
Package	HV400		**Assembly Site**	HVVi	Phoenix, Arizona
Technology	HVVFET™		**Final Test Site**	HVVi	Phoenix, Arizona

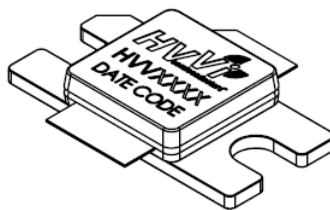

Figure 1. Package drawing of the HVV1011-300.

Table 2. List of reliability lab companies, locations, and tests performed.

Reliability Lab	Location	Tests Completed
ON Semiconductor Reliability Lab	Phoenix, Arizona	HTGB, HTRB, UHAST, Solderability, RSH
Evans Analytical Group	Fremont, California	Temperature Cycle
Silicon Cert, Ltd.	Pennsylvania	Mechanical Shock, Variable Vibration Frequency, Constant Acceleration

Qualification Tests and Results

The qualification tests were performed per standard test conditions (JEDEC, AEC-101, MIL-STD-883). Sample sizes were chosen per recommended sizes or per Lot Tolerance Percent Defective (LTPD) Sampling based on the Military Standards (5% level).

Table 3. A list of reliability tests completed for the HVV1011-300 qualification.

Stress	Abbv.	Ref.	Conditions	Duration/ Acceptance	Lot A	Lot B	Lot C
Electrical Parameter Assessment	ED	JESD86	Datasheet	Per datasheet	All	All	All
High Temperature Reverse Bias	HTRB	JESD22-A108, JESD85	80% of BVds (max) (76 V)	1008 hr / 0 Fail	0/45	0/45	0/45
High Temperature Gate Bias	HTGB	JESD22-A108, JESD85	100% of Vgs (max) (6 V)	1008 hr / 0 Fail	0/45	0/45	0/45
Temperature Cycling	TC	JESD22-A104	-40 °C to +125 °C	1000 cycles / 0 Fail	0/45	0/45	0/45
Temperature/Humidity (Unbiased)	UHAST	JESD22-A118	+130 °C, 85% RH	96 hours / 0 Fail	0/45	0/45	0/45
Thermal Resistance Measurements (Average & Pulsed)	θ_{JC}	JESD24-3	Under spec operating conditions	Characterize device	0/5	0/5	0/5
Solderability	SD	JESD22-B102E	Per std	0 Fail	0/15		
Resistance to Solder Heat	RSH	JESD22-B106C	Per std	0 Fail	0/30		
Variable Vibration Frequency	VVF	JESD22-B103	20 – 2000 Hz, Peak force = 20 g	4 min with 4 travels per axis / 0 fail	0/5		
Mechanical Shock	MS	JESD22-B104	Accel = 1500 g; Duration = 0.5 msec	5 times in both directions of 3 axis (6 directions total) / 0 Fail	0/5		
Constant Acceleration	CA	MIL-STD-833-2001	10000 g	Y1 Direction	0/6		

Explanation of Tests

Stress Test/Specification: High Temperature Reverse Bias (HTRB)/JESD-A108, JESD85
Conditions: Tj = 150 °C; Biased at 80% of reverse bias voltage rating
Read Points: 0, 168, 504, and 1008 hours
Sample Size: 3 lots, 45 units each (per LTPD 5% level with no failures)
Purpose: Accelerate failure mechanisms by applying high temperature and specified voltage conditions over an extended period of time.
Possible Failure Mechanisms/Modes: The main failure mechanism is the degradation of the break down voltage due to mobile ions or contaminates which form a leakage path. The failure mechanism can be accelerated by temperature and potential (voltage). The failure modes are seen as parametric shifts in leakage and gain or catastrophic failure. Electrical parameters affected include Vbr(dss), Idss, Vgs, and Gp.

Stress Test/Specification: High Temperature Gate Bias (HTGB)/JESD-A108, JESD85
Conditions: Tj = 150 °C; Biased at 100% of gate voltage rating
Read Points: 0, 168, 504, and 1008 hours
Sample Size: 3 lots, 45 units each (per LTPD 5% level with no failures)
Purpose: Accelerate failure mechanisms by applying high temperature and specified voltage conditions over an extended period of time.
Possible Failure Mechanisms/Modes: The main failure mechanisms are the rupture or degradation of the gate oxide due to oxidation issues such as oxide structure abnormalities, oxide thickness variations, contamination or particulates in or on the gate oxide, and channel inversion due to mobile ions in the gate oxide. The failure mechanisms can be accelerated by temperature and potential (voltage). Failure modes include parametric shifts and catastrophic failure. Electrical parameters affected include Igss, Idss, and Vgs.

Stress Test/Specification: Temperature Cycling (TC)/JESD22-A104
Conditions: Ta = -40 °C to +125 °C; unbiased
Read Points: 0, 100, 500, and 1000 cycles
Sample Size: 3 lots, 45 units each (per LTPD 5% level with no failures)
Purpose: Accelerate failure mechanisms caused by cycling between high and low temperatures.
Possible Failure Mechanisms/Modes: Failure mechanisms include fatigue and cracking related failures such as broken bonds or cracked die due to stresses caused by thermal mismatches in Coefficients of Thermal Expansion (CTE). Failure modes include degradation of thermal and electrical characteristics and catastrophic failure. Thermal and electrical parameters affected include Rdson, R(θ)jC, Vdss, and Vgs.

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Stress Test/Specification: Unbiased Highly Accelerated Stress Test (UHAST)/JESD22-A118
Conditions: Ta = 131 °C, 85% R.H.; unbiased
Read Point: 0 and 96 hours
Sample Size: 3 lots, 45 units each (per LTPD 5% level with no failures)
Purpose: Accelerate failure mechanisms caused by extreme conditions of temperature and humidity which cause moisture ingress into the package.
Possible Failure Mechanisms/Modes: Failure mechanisms include contamination, corrosion, and chemical reactions caused by moisture ingress into the package. Moisture ingress can be along the package-to-lead interface or through an inadequate package seal. The failure mechanisms can be accelerated by temperature and humidity. Failure modes include parametric shifts or catastrophic failure. Electrical parameters affected include Vbr(dss), Idss, and Igss.

Stress Test/Specification: Resistance to Solder Heat (RSH)/JESD22-B106C
Conditions: Per standard.
Sample Size: 1 lot, 30 units
Purpose: Determine the ability of a device to withstand temperatures encountered in wave soldering or board assembly operations.
Possible Failure Mechanisms/Modes: A failure mechanism is inadequate package design. Failure modes include parametric shifts, catastrophic failure, and mechanical failure of the package.

Stress Test/Specification: Solderability (SD)/JESD22-B102E
Conditions: Per standard.
Sample Size: 1 lot, 15 units
Purpose: Evaluate the ability of the component leads and/or package terminations to be wetted and produce an adequate fillet when coated with solder.
Possible Failure Mechanisms: Failure mechanisms include contamination on the package terminations/leads or other plating anomalies. Failure modes include solder voids, pinholes, and inadequate wetting of the leads and/or package terminations.

Stress Test/Specification: Vibration, Variable Frequency/JESD22-B103
Conditions: 20 – 2000 Hz, Peak force = 20 g
Sample Size: 1 lot, 5 units
Purpose: Evaluate a device when subjected to vibration in a specified frequency range.
Possible Failure Mechanisms: Failure mechanisms include fatigue, fracture, wear, corrosion fatigue, and stress corrosion cracking. Failure modes include degradation of operating characteristics, catastrophic failure, or mechanical damage similar to that resulting from excessive vibration.

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Stress Test/Specification: Mechanical Shock (MS)/JESD22-B104
Conditions: Acceleration = 1500 g, Duration = 0.5 msec
Sample Size: 1 lot, 5 units
Purpose: Evaluate a device subjected to moderately severe shocks as a result of sudden applied forces or abrupt changes in motion which simulate heavy usage, transportation, or field applications.
Possible Failure Mechanisms/Modes: Failure mechanisms include fatigue, fracture, wear, corrosion fatigue, and stress corrosion cracking. Failure modes include degradation of operating characteristics, catastrophic failure, or mechanical damage similar to excessive vibration, particularly if the shock pulses are repetitive.

Stress Test/Specification: Constant Acceleration (CA)/MIL-STD-883 Method 2001
Conditions: 10000 g, six axial directions
Sample Size: 1 lot, 6 units
Purpose: Evaluate structural and mechanical weaknesses not necessarily detected in shock and vibration testing. Mechanical limitations of the package can be assessed including the internal metallization and lead system, the die or substrate attachment, and other structures of the device.
Possible Failure Mechanisms/Modes: Failure mechanisms include fatigue, fracture, wear, corrosion fatigue, and stress corrosion cracking. Failure modes include degradation of operating characteristics, catastrophic failure, or mechanical damage similar to that resulting from excessive vibration, particularly if the shock pulses are repetitive.

Qualification by Similarity

The following devices are qualified by similarity to the HVV1011-300 based on similarity in wafer technology, fabrication, die size, assembly manufacturing, and materials:
HVV1012-250, HVV0608-175, HVV0405-175, HVV0912-150, HVV1214-100.

Summary

The reliability test results documented herein qualify the HVV1011-300 device and the HV400 package. The die is supplied by ON Semiconductor's COM1 facility in Phoenix, Arizona and the package is assembled at HVVi in Phoenix, Arizona. The HVV1011-300 device meets or exceeds HVVi's requirements for product reliability.

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