

Special Feature

Military-Specific I/O

Power Transistor Advances Enhance Military Radar Designs

The pressure is on for military radar and avionics systems developers to boost performance while reducing system size. A new RF power transistor architecture helps smooth the way.

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Military avionics and radar design has seen profound changes over the past few decades. New multi-mode systems now allow radar to simultaneously track air and sea targets while continuously scanning an operational area. New signal processing techniques such as pulse compression increase resolution while maintaining range. Ground-based radar (GBR) systems operating in the 1.2 GHz to 1.4 GHz band offer better range and visibility than they ever have before.

Among the key driving forces behind these continual improvements in ground and aircraft-based primary and secondary radar systems has been developers' ability to improve power amplifier (PA) performance. Military radar and avionics systems developers are under constant pressure to maximize performance and efficiency while reducing component count, board and system footprint. Over the last several decades, the constant evolution of the RF power transistor, and its impact on PA design, has played a crucial role in this process. By continually improving RF transistor performance, military avionics and radar system designers have been able to deliver PAs capable of providing higher levels of power at higher efficiency and with higher linearity. Figure 1 shows a radar antenna system aboard the aircraft carrier USS Abraham Lincoln.



Figure 1

Through continuous improvements of RF transistor performance, radar designers have been able to get higher levels of power at higher efficiency and with higher linearity. Shown here is the SPS-49 air search radar antenna mounted atop the lattice mast aboard the nuclear-powered aircraft carrier USS Abraham Lincoln.

Constant Improvement

Back in the 1950s and 1960s, early development efforts of power transistors for RF applications centered on the use of Germanium. By the mid-1960s, however, military designers had largely migrated to bipolar components that offered high power in a cost-effective and familiar fabrication process. As performance de-

mands increased in the 1970s, developers in the commercial markets moved to double-diffused Metal Oxide Semiconductors (DMOS). This new architecture used a vertical transistor design to support operating voltages from 28V to 50V at frequencies up to 500 MHz. Combining fast switching response, better thermal stability, higher input impedance

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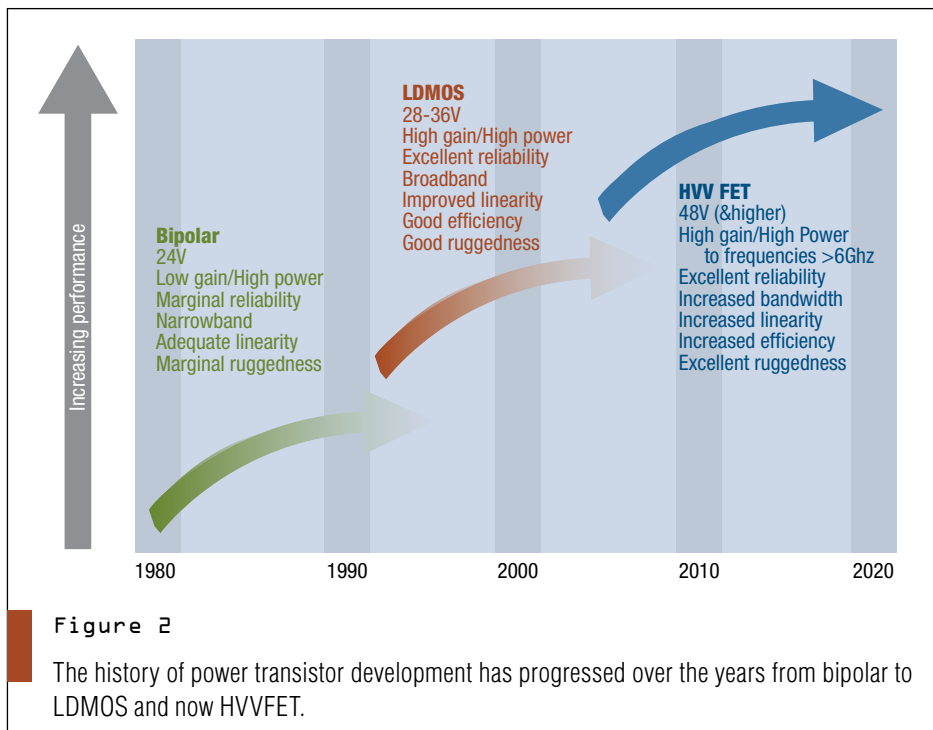
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and simpler circuit architecture, DMOS was widely adopted.

As commercial communications systems developers began building out the wireless infrastructure in the 1980s, escalating performance demands drove researchers to explore alternative strategies capable of meeting the higher power efficiencies required for PAs in base stations. Driving this effort were inherent limitations to the DMOS architecture. Wireless base station designers needed PAs capable of offering higher linearity to satisfy higher-order modulation schemes, greater average output power levels, broader operating bandwidths and lower system operating costs through higher power efficiency. To address this challenge, developers introduced the Lateral Double-diffused metal Oxide Semiconductor (LDMOS) power transistor. Figure 2 traces the history of power transistor development.

Despite these continual improvements in power transistor design, each architecture currently available brings with it significant limitations. Bipolar devices offer relatively high power density at high voltage levels, but with limited gain. Newer LDMOS alternatives promise improved gain and better efficiency, but with limited ruggedness. Power transistors fabricated in non-silicon technologies such as Gallium Nitride or

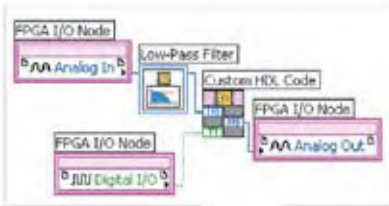
Silicon Carbide deliver better performance through the technology's higher inherent electron mobility, at a significantly higher cost and with limited reliability.

Beyond Bipolar

Given the relatively long design cycles in the military market and the need for relatively high power and high reliability, most military designers have opted for bipolar devices to meet their design needs. Still, military designers are not immune to the same forces driving commercial radar designs. Developers of today's aircraft-mounted military radar systems are facing escalating pressure to reduce the size, weight and power consumption of their systems without sacrificing reliability or increasing cost. On the ground-based side, military system designers need solutions capable of delivering higher levels of output power without compromising efficiency or operational cost. In both cases, high reliability is a must. Clearly military system designers need a new approach to power transistor design that can be used to develop PAs with higher power density in smaller packages, while retaining high levels of ruggedness.

Recently, engineers at HVVi Semiconductors announced the first major advance in power transistor design since the development of LDMOS over 15 years ago. This

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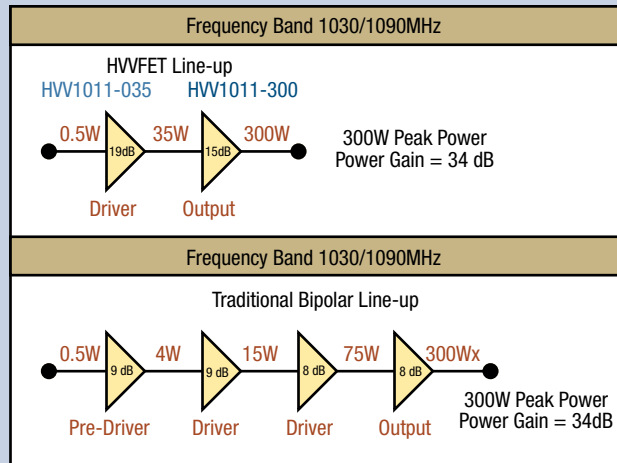


Figure 3

By offering more than twice the gain of comparable bipolar devices, power transistors using this new technology can dramatically reduce drive stage requirements. The Figure shown here compares a traditional bipolar transistor lineup to a lineup using the HVVFET. Shown here is a typical 300W solution for IFF applications in the 1030 to 1090 MHz band. Designers using traditional lower gain bipolar components would need to configure four stages of devices. Using easy-to-match 48V components based on the HVVFET architecture, designers can generate the same power using a 35W device offering 19 dB of gain to drive a 300W transistor providing 15 dB of gain.

By delivering 600W of power at 30 percent better system efficiency, a two-stage design reduces system power supply requirements and operating costs. The HVVFET-based design not only eliminates two driver stages, it also eliminates all of the capacitors in the RF interstage matching as well as a variety of supporting external components. PCB footprint requirements shrink by at least one-third and system costs drop proportionally.

new approach uses a High Voltage Vertical Field Effect Transistor (HVVFET) to support higher power levels through voltage. By reducing parasitic capacitances, this new topology is capable of 3X the frequency of LDMOS devices with a 30 percent boost in system power efficiency. Compared to the lateral transistor used in LDMOS, the vertical approach used in the HVVFET offers significantly higher power density, allowing component designers to deliver twice the power in the same package. Ultimately, designers believe this new architecture will support devices up to 150V and operation all the way up to 12.5 GHz.

Just as important to military system designers, this new architecture offers major advances in system ruggedness and reliability. The vertical structure of the HVVFET allows designers to develop transistors that deliver higher voltage while generating less heat. Heat is a major impediment to power amplifier performance and poses a primary threat to reliability. In a lateral power tran-

sistor like that used in LDMOS, the hottest part of the transistor is located approximately 100 microns from the heat sink. The heat dissipated by the device must pass through the entire thickness of the die.

Closer to the Heat Sink

In this new vertical design, the hottest point on the die is located less than 5 microns from the heat sink. That difference offers dramatic heat extraction advantages. Moreover, to better manage thermal performance, engineers at HVVi have bumped the die that rapidly dissipates the heat. As a result, power transistors built using this new architecture offer substantially better reliability. HVVi's first products, for example, are specified to withstand a VSWR of 20:1 at all phase angles under full rated output power or about 10x as high as bipolar devices and 25x the rating of LDMOS devices.

The HVVFET architecture's ability to scale to higher voltages offers unique

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advantages. The architecture depletes vertically into the substrate as voltage is applied to the drain. The architecture approaches planar breakdown in the vertical drain region and thereby stands off the maximum voltage with the minimum $R_{ds(on)}$. At the same time the architecture maximizes packing density while minimizing parasitic capacitance.

The architecture was designed so that performance characteristics improve as the device moves to higher operating voltages. For a higher voltage at a fixed RF power, the drain-source current of the device decreases. This allows power transistor designers to reduce die size and decrease parasitic capacitance per watt. Lower capacitance supports higher frequency operation and lower current improves system reliability.

System Implications

The most important advantages of this new architecture, however, come not at the individual device level, but at the system level. Figure 3 compares a traditional bipolar transistor lineup to a lineup using the HVVFET. One system advantage is that the lower current requirements associated with a higher voltage supply and lower thermal resistance improve system reliability and extend the system lifecycle. Moreover, since HVVFET transistors are specified to withstand a 20:1 VSWR at all phase angles under full rated out-

put power, the new smaller design offers higher reliability. For airborne L-band applications such as these, fewer components also translate into less weight. Moreover, the technology's significantly higher VSWR rating may allow designers to eliminate the use of isolators and, in the process, further reduce system weight and cost. Finally, a simpler design with fewer components translates into simpler system architecture and the expenditure of fewer design resources.

Similar advantages are achievable in ground-based radar applications. Figure 4 shows an HVVFET-based configuration for L-band pulsed radar applications in the 1.2 to 1.4 GHz frequency band. In the HVVFET configuration, a 25W device with 18 dB of gain drives a pair of 100W transistor providing 19 dB of gain. The lineup provides 200W of power at over 47% efficiency. Again, by reducing amplification stages, the designer earns major improvements in system footprint, cost and reliability.

Constant Trade-Off

Power amplifier design is a constant trade-off among performance attributes. Historically, designers have had to balance improvements in power output or gain against limitations in linearity or efficiency. The continual evolution of silicon RF power transistors is gradually undermining that perception however. With

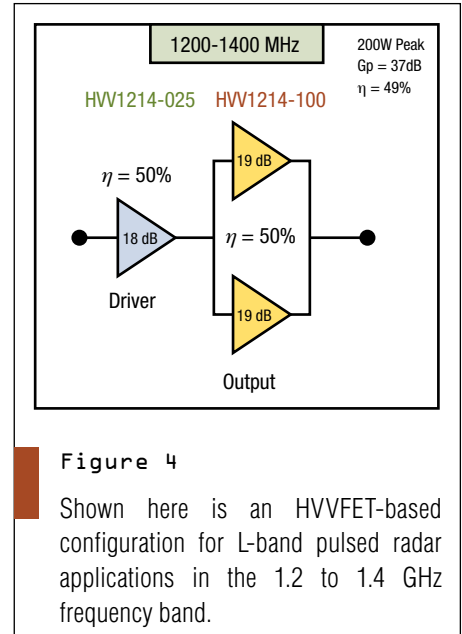


Figure 4

Shown here is an HVVFET-based configuration for L-band pulsed radar applications in the 1.2 to 1.4 GHz frequency band.

each new generation developers have been able to tweak architectures to meet new performance requirements. The latest development in RF power transistors with the HVVFET architecture promises to deliver higher power density, efficiency and reliability levels to next-generation military radar and avionics system. ■■

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